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UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/829,793	04/10/2001	Martijn Johannes Lambertus Emons	NL 000215	1893

			EXAMINER
24738	7590	01/28/2005	KIM, HONG CHONG

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
1109 MCKAY DRIVE, M/S-41SJ
SAN JOSE, CA 95131

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>08 December 2004</u>.
2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>6-8</u> is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) <u>6-8</u> is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All   b)☐ Some * c)☐ None of:
        1.☐ Certified copies of the priority documents have been received.
        2.☐ Certified copies of the priority documents have been received in Application No. _____.
        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

Detailed Action

1.   Claims 6-8 are presented for examination.   This office action is in response to

the RCE amendment filed on 12/08/2004.

2.   The examiner requests, in response to this Office action, any reference(s) known

to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention

as defined by the independent and dependent claims. That is, any prior art (including

any products for sale) similar to the claimed invention that could reasonably be used in

a 102 or 103 rejection. This request does not require applicant to perform a search.

This **request** is not intended to interfere with or go beyond that **required** under 37

C.F.R. 1.56 or 1.105.

        The request may be fulfilled by asking the attorney(s) of record handling

prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple

statement that the query has been made and no prior art found is sufficient to fulfill the

request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are

waived for those documents submitted in reply to this request. This waiver extends only

to those documents within the scope of this request that are included in the application's

first complete communication responding to this requirement. Any supplemental replies

subsequent to the first communication responding to this request and any information

disclosures beyond the scope of this are subject to the fee and certification

requirements of 37 CFR section 1.97.

        In the event prior art documentation is submitted, a discussion of relevant

passages, figs. etc. with respect to the claims is requested. The examiner is looking for

specific references to 102/103 prior art that identify independent and dependent claim

limitations. Since applicant is most knowledgeable of the present invention and

submitted art, his/her discussion of the reference(s) with respect to the instant claims is

essential. **A response to this inquiry is greatly appreciated.**

The examiner also requests, in response to this Office action, support be

shown for language added to any original claims on amendment and any new claims.

That is, indicate support for newly added claim language by specifically pointing to

page(s) and line number(s), in the specification and/or drawing figure(s). This will assist

the examiner in prosecuting the application.

Claim Rejections - 35 USC § 102/103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3.   Claims 6-8 are rejected under 35 U.S.C. 102(b) as being unpatentable over

Fuller US Patent 5,632,038 or, in the alternative, under 35 U.S.C. 103(a) as being

unpatentable over Fuller US Patent 5,632,038 in view of Yamahata US Patent No.

5,247,639.

As to claim 6, Fuller discloses a cache interface circuit, comprising: a processor

interface (Fig. 1 lines between processor and cache controller and col. 3 lines 10-12,

col. 4 lines 11-12, & col. 4 lines 52-53); a main memory interface (Fig.1 lines between

system memory and cache controller and col. 3 lines 10-12); a cache memory interface

(Fig. 1 lines between cache memory and cache controller and col. 3 lines 10-12); a

cache-bypass mode control signal input (col. 3 lines 25-28) for said processor to

indicate a cache bypass mode, in response to a programmer instruction inserted in a

program being executed by the processor (col. 4 lines 33-35, a control and power

management logic (Fig. 2 Ref. 60) is controlled by the processor (Fig. 2 Ref. 50) and

operates according to instructions and data stored in a ROM 65. In other words, the

instructions stored in ROM or firmware (col. 4 line 36, since ROM or firmware contains

instruction to be executed by a processor) are executed by the processor to control the

cache memory power) explicitly for the purpose of switching to cache by pass in which

cache bypass mode memory access requests are served from said main memory; a

power control output for switching off (col. 6 line 10, turn the cache off reads on this

limitation) operating power to said cache memory.

Even if in response to a programmer instruction inserted in a program being

executed by the processor explicitly for the purpose of switching to cache by pass in

which cache bypass mode memory access requests are served from said main memory

does not specifically discloses by the Fuller.

Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Fuller US Patent 5,632,038 in view of Yamahata US Patent No. 5,247,639.

Fuller discloses a cache interface circuit, comprising: a processor interface (Fig.

1 lines between processor and cache controller and col. 3 lines 10-12, col. 4 lines 11-

12, & col. 4 lines 52-53); a main memory interface (Fig.1 lines between system memory and cache controller and col. 3 lines 10-12); a cache memory interface (Fig. 1 lines between cache memory and cache controller and col. 3 lines 10-12); a cache-bypass mode control signal input (col. 3 lines 25-28 and col. 4 lines 23-25 & 33-39); a power control output for switching off (col. 6 line 10, turn the cache off reads on this limitation).

Eve if Fuller does not specifically disclose a cache-bypass mode control signal input, in response to a programmer instruction inserted in a program being executed by the processor explicitly for the purpose of switching to cache by pass in which cache bypass mode memory access requests are served from said main memory.

It was common knowledge in memory art to send an instruction to bypass a cache. For example, Yamahata discloses a cache-bypass mode control signal input (col. 2 lines 22-26, command reads on this limitation since command is a part of instruction from a processor), in response to a programmer instruction inserted in a program being executed by the processor explicitly for the purpose of switching to cache by pass in which cache bypass mode memory access requests are served from said main memory (col. 2 lines 22-26, command reads on this limitation since command is a part of instruction from a processor) for the purpose of increasing processing speed and saving power.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a cache-bypass mode control signal input, in response to a programmer instruction inserted in a program being executed by the processor explicitly for the purpose of switching to cache by pass in which cache

bypass mode memory access requests are served from said main memory as shown in

Yamahata into the invention of Fuller for the advantages stated above.

As to claim 7, Fuller further discloses a cache bypass mode program instruction

interceptor connected to the processor interface and providing for switching between

said cache and cache bypass modes without having received an explicit signal to do so

at he cache bypass mode control signal input wherein said processor need not take any

action to switch between said cache and cache-bypass modes (Fig. 2 Ref. 60, separate

control and power management logic reads on this limitation).   Yamahata further

discloses a cache bypass mode program instruction interceptor connected to the

processor interface and providing for switching between said cache and cache bypass

modes without having received an explicit signal to do so at he cache bypass mode

control signal input wherein said processor need not take any action to switch between

said cache and cache-bypass modes (col. 2 lines 22-26 and Fig. 2 Refs. 220 & 212).

As to claim 8, Fuller further discloses a sequence of program instruction disposes

in said main memory (system memory, col. 4 line 48-50 and instructions, col. 4 line 25

read on this limitation, since an instruction or a program is loaded into the system

memory and executed by a processor sequentially) that require execution by the

processor in said cache mode (col. 5 lines 23-35) and that are bracketed by program

instructions acted on by the cache-bypass mode program instruction (col. 4 lines 23-

35).   Yamahata further discloses a sequence of program instruction (Fig. 2 Refs. 220 &

212) disposes in said main memory (col. 2 lines 22-26, instructions read on this

limitation, since an instruction or a program is loaded into the main memory and

executed by a processor sequentially).

Response to Amendment

4.   Applicant's arguments filed on 12/8/2004 have been fully considered but they are

not persuasive.

Applicant's argument on page 4 that the reference does not disclose a cache-

bypass mode control signal input, in response to a programmer instruction inserted in a

program being executed by the processor explicitly for the purpose of switching to

cache by pass in which cache bypass mode is not considered persuasive.

Fuller discloses a cache-bypass mode control signal input (col. 3 lines 25-28) for

said processor to indicate a cache bypass mode, in response to a programmer

instruction inserted in a program being executed by the processor (col. 4 lines 33-35, a

control and power management logic (Fig. 2 Ref. 60) is controlled by the processor (Fig.

2 Ref. 50) and operates according to instructions and data stored in a ROM 65. In other

words, the instructions stored in ROM or firmware (col. 4 line 36, since ROM or firmware

contains instruction to be executed by a processor) are executed by the processor to

control the cache memory power via a control and power management logic) explicitly

for the purpose of switching to cache by pass in which cache bypass mode memory

access requests are served from said main memory; a power control output for

switching off (col. 6 line 10, turn the cache off reads on this limitation) operating power

to said cache memory.

Yamahata also discloses a cache-bypass mode control signal input, in response

to a programmer instruction inserted in a program being executed by the processor

explicitly for the purpose of switching to cache by pass in which cache bypass mode

memory access requests are served from said main memory (col. 2 lines 22-26,

command reads on this limitation since command is a part of instruction from a

processor) for the purpose of increasing processing speed and saving power.

Therefore broadly written claims are disclosed by the references cited.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure

A shortened statutory period for response to this action is set to expire 3 (three) months

and 0 (zero) days from the mail date of this letter. Failure to respond within the period

for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP

710.02, 710.02(b)).

When responding to the office action, Applicant is advised to clearly point out the

patentable novelty which he or she thinks the claims present in view of the state of the

art disclosed by the references cited or the objections made. He or she must also show

how the amendments avoid such references or objections.   See 37 C.F.R. ' 1.111(c).

When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong C Kim whose telephone number is 703-272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (703) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
703-872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121
Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).
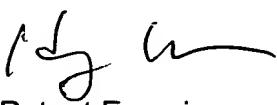
HK
Primary Patent Examiner
January 27, 2005